A 130 nm Generation Logic Technology Featuring 70 nm Transistors, Dual V_T Transistors and 6 Layers of Cu Interconnects

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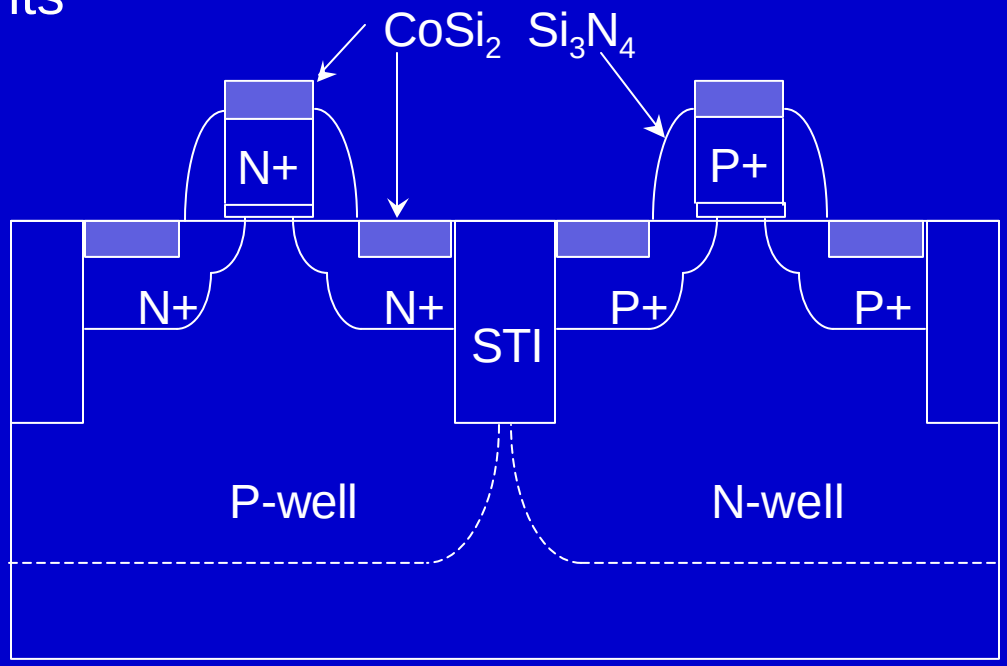
Outline

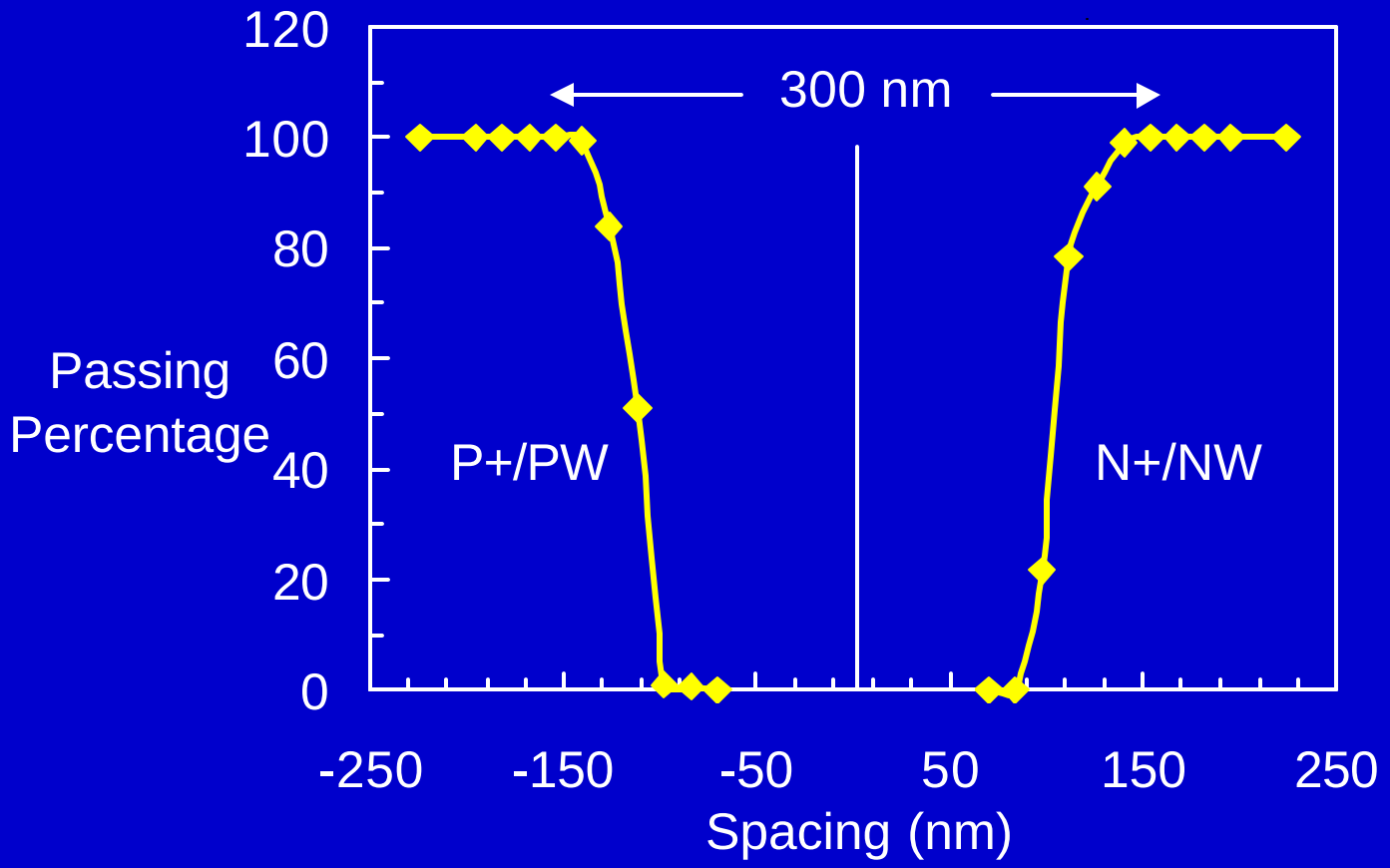
- Front End Technology Features
- Transistor Performance
- Interconnect Features
- SRAM Results
- Conclusions

Front End Process Flow and Features

- Shallow Trench Isolation
- Well & V_T Adjust Implants
- Gate Oxide Formation
- Poly Gate Patterning
- Shallow Source Drain Extensions
- Halo Implants
- Si_3N_4 Spacer
- Deep Source/Drain
- Co Salicide

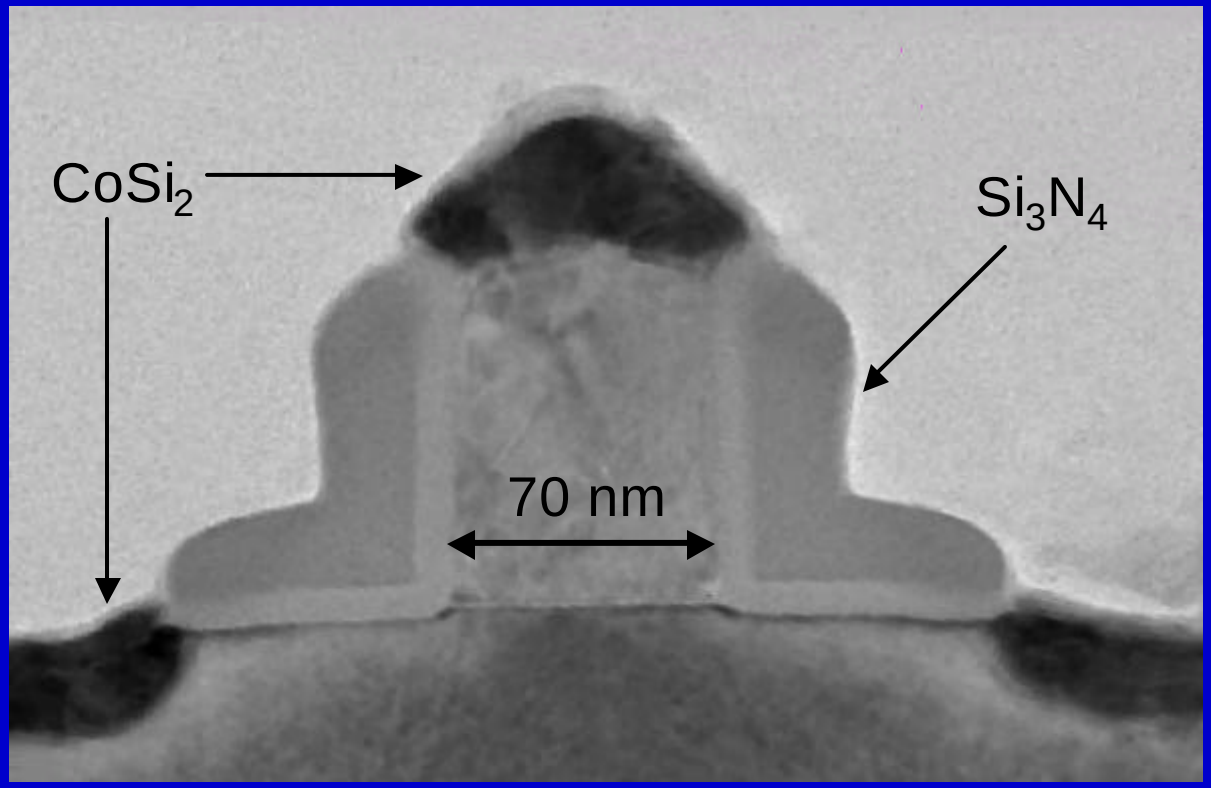


Shallow Trench Isolation



Robust N+ to P+ isolation down to 300 nm.
STI Pitch of 364 nm and trench depth of 450 nm

70 nm Gate Length MOSFET



Junction Area Capacitance

	C_{JA} N+/PW	C_{JA} P+/NW
This Work	0.60	0.60
Diaz, VLSI '00	0.90	1.20
Imai, IEDM '99	0.82	1.10
Mehrotra, IEDM '99	1.10	0.80
Yeap, VLSI '00	1.22	1.41
Yoshimura, VLSI '00	1.10	0.75
	$fF/\mu m^2$	$fF/\mu m^2$

C_{JA} significantly lower than recent high performance technologies

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Dual V_T Transistors

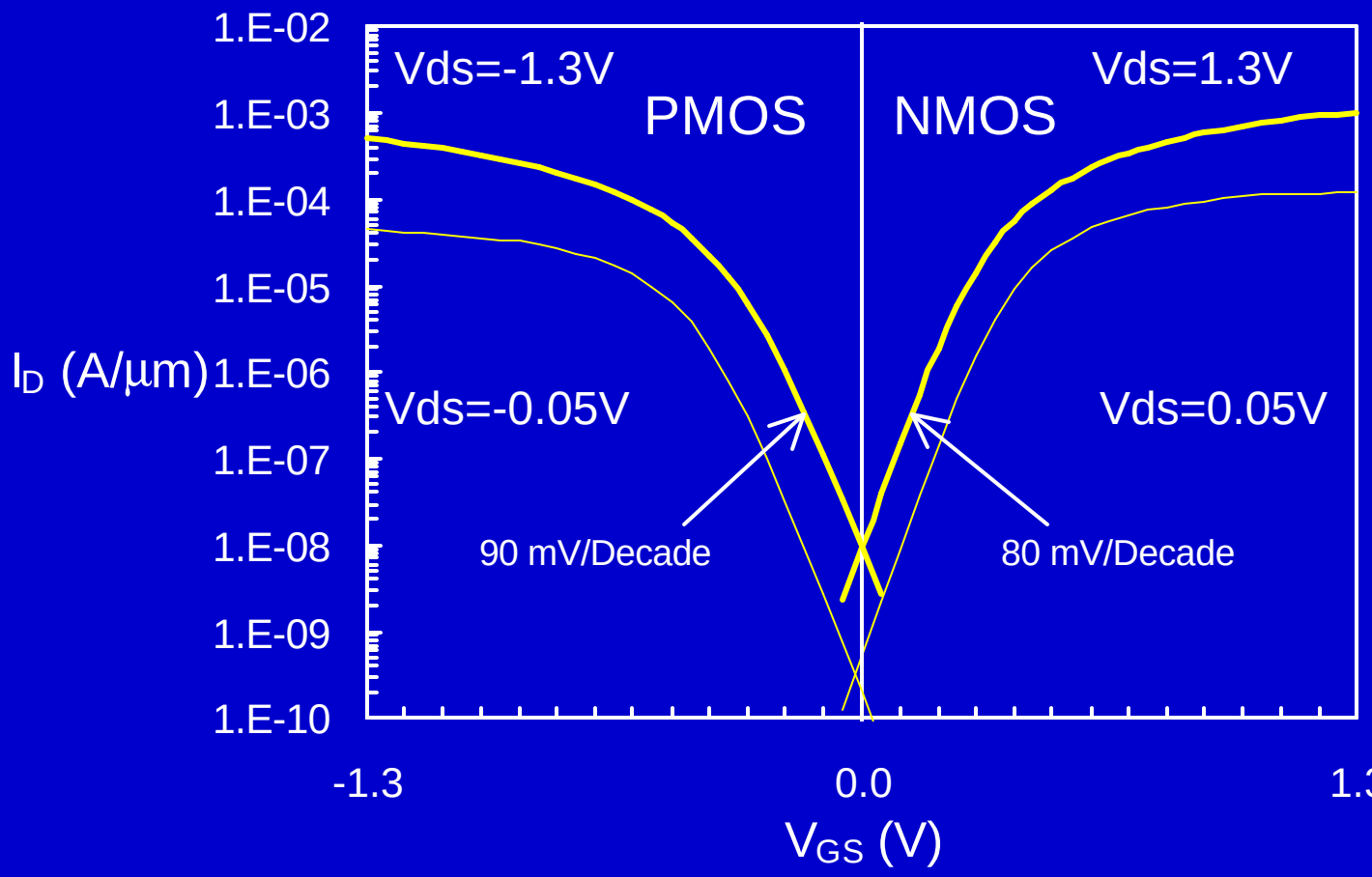
- Dual V_T devices provide circuit design flexibility to optimize performance vs. leakage power
- High V_T devices used for most circuits and maintain low leakage power
- Low V_T devices used selectively in speed critical paths

Transistor Parameters

	0.18 µm [1]		0.13 µm		
	NMOS	PMOS	NMOS	PMOS	
V_{DD}	1.5	1.5	1.3	1.3	V
L_{GATE}	100	100	70	70	nm
T_{OX}	2.0	2.0	1.5	1.5	nm
I_{OFF} (high V_T)	3	3	10	10	nA/µm
I_{OFF} (low V_T)	-	-	100	100	nA/µm
I_{DSAT} (high V_T)	1.04	0.46	1.02	0.50	mA/µm
I_{DSAT} (low V_T)	-	-	1.17	0.60	mA/µm

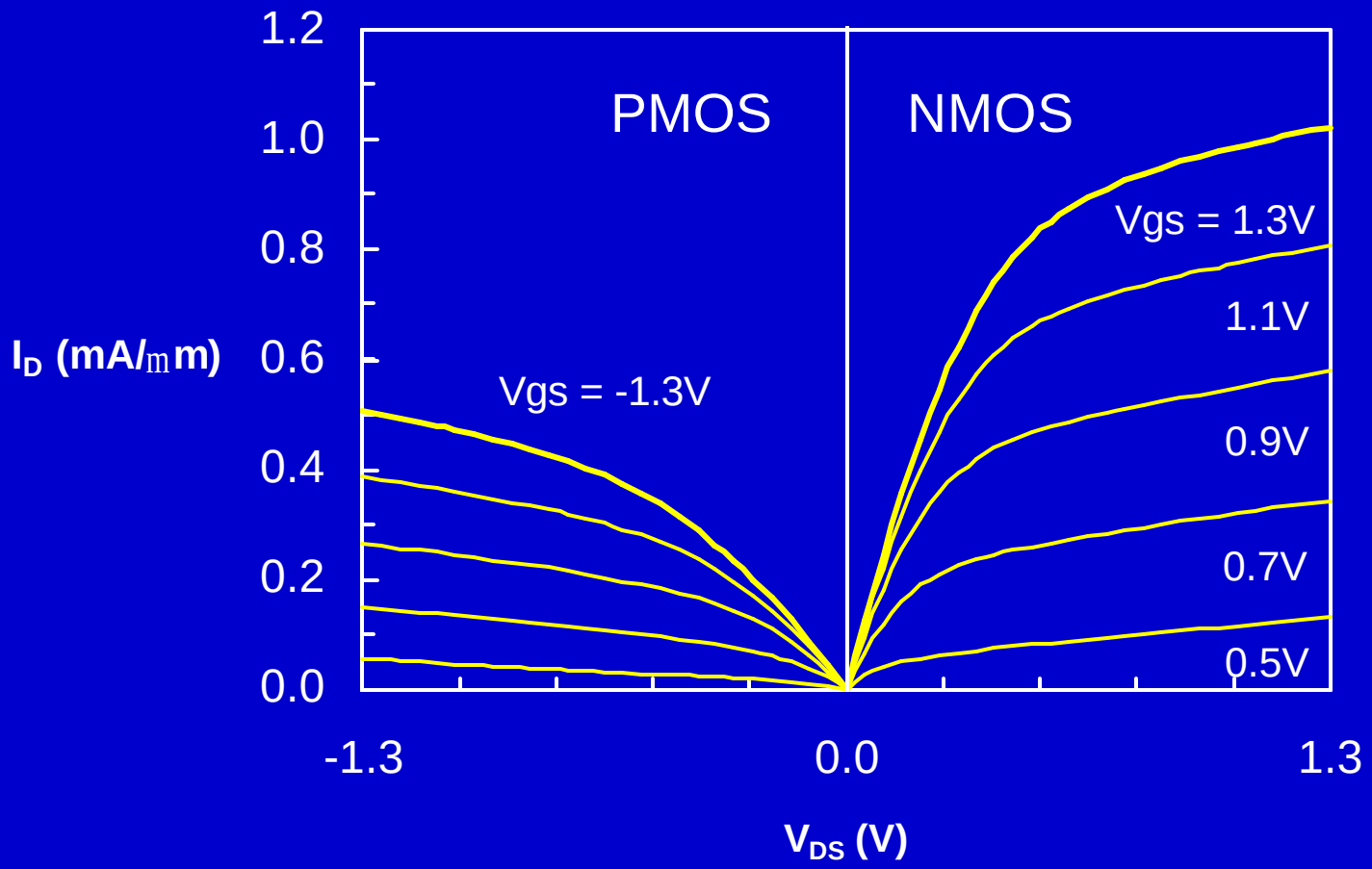
[1] T. Ghani, 1999 IEDM

High V_T Sub-threshold Curves, L_G = 70 nm



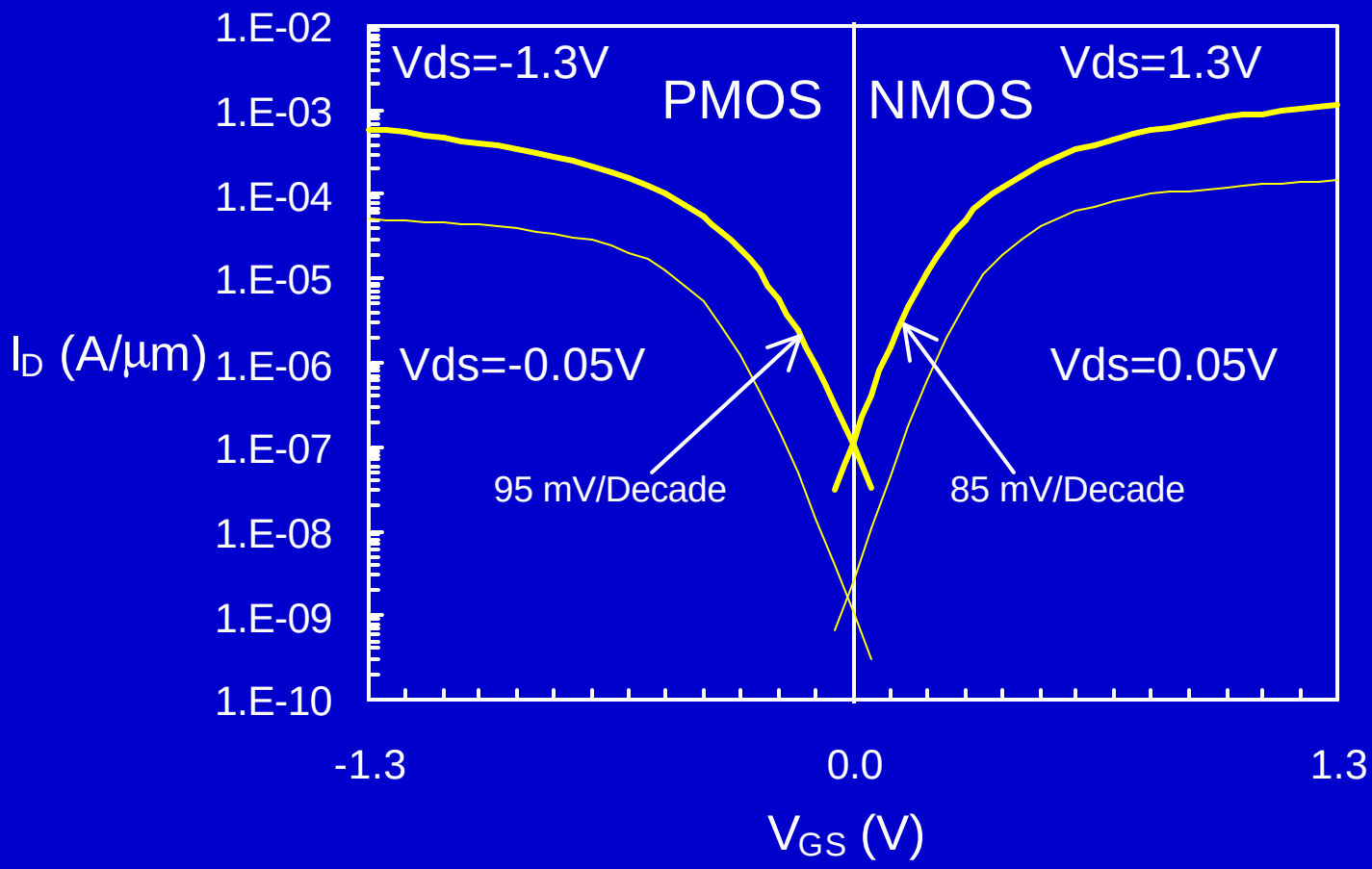
Off current = 10 nA/mm, Sub-threshold slopes < 90 mV/decade

High V_T I-V Curves, L_G = 70 nm



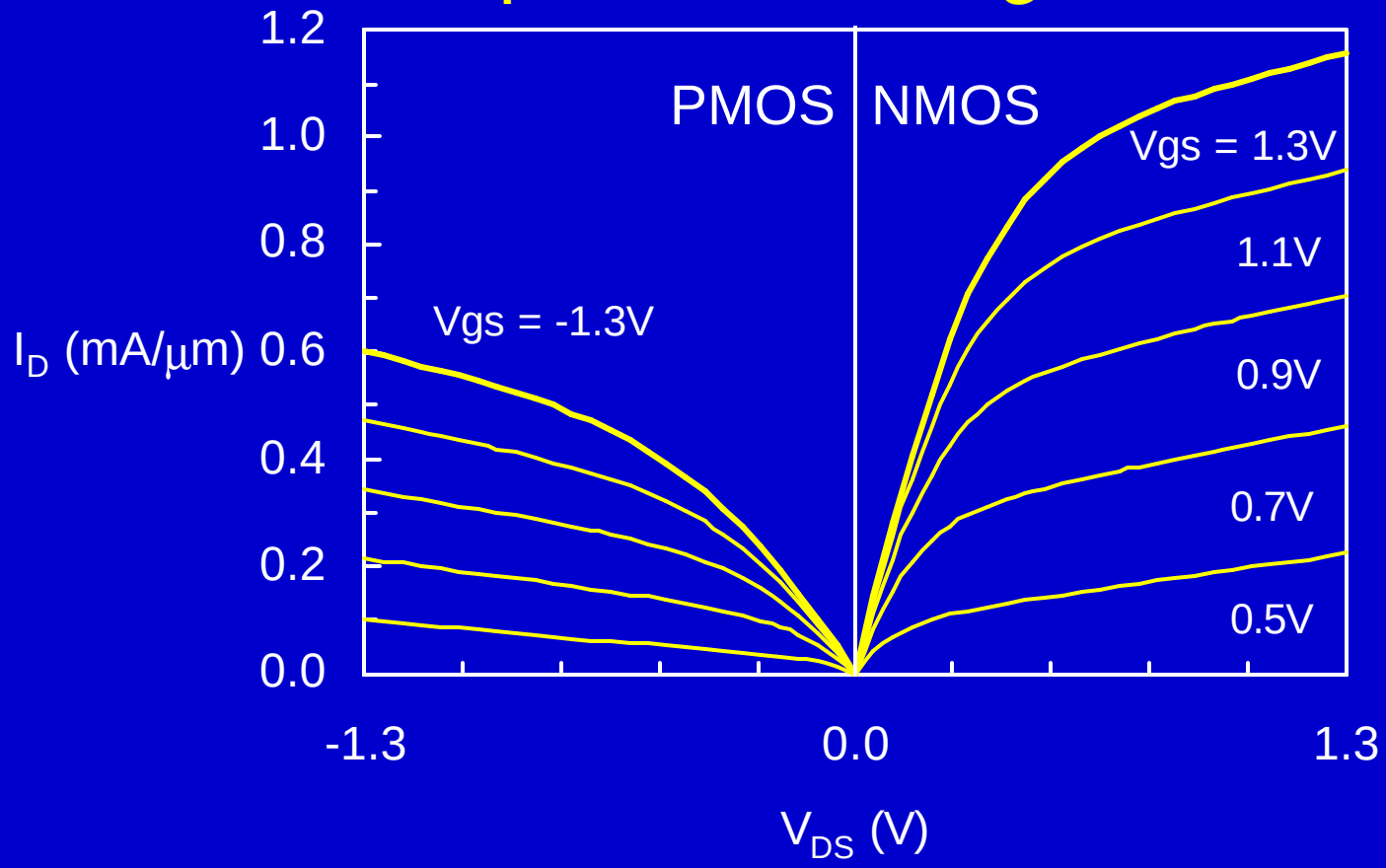
PMOS I_{DSAT} = -0.5 mA/mm NMOS I_{DSAT} = 1.02 mA/mm

Low V_T Sub-threshold Curves, L_G = 70 nm



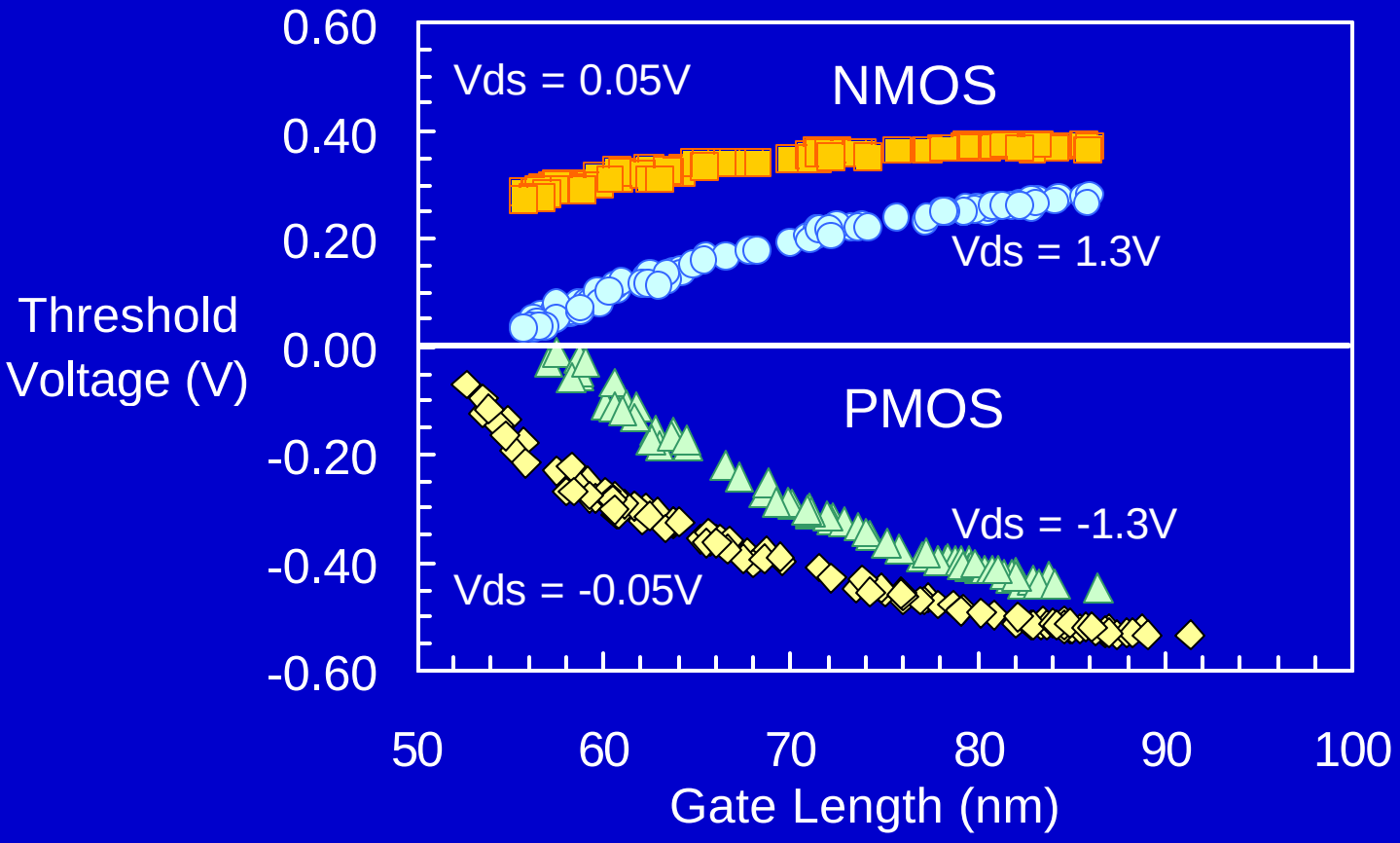
Off current = 100 nA/mm, Sub-threshold slopes < 95 mV/decade

Low V_T I-V Curves, L_G = 70 nm



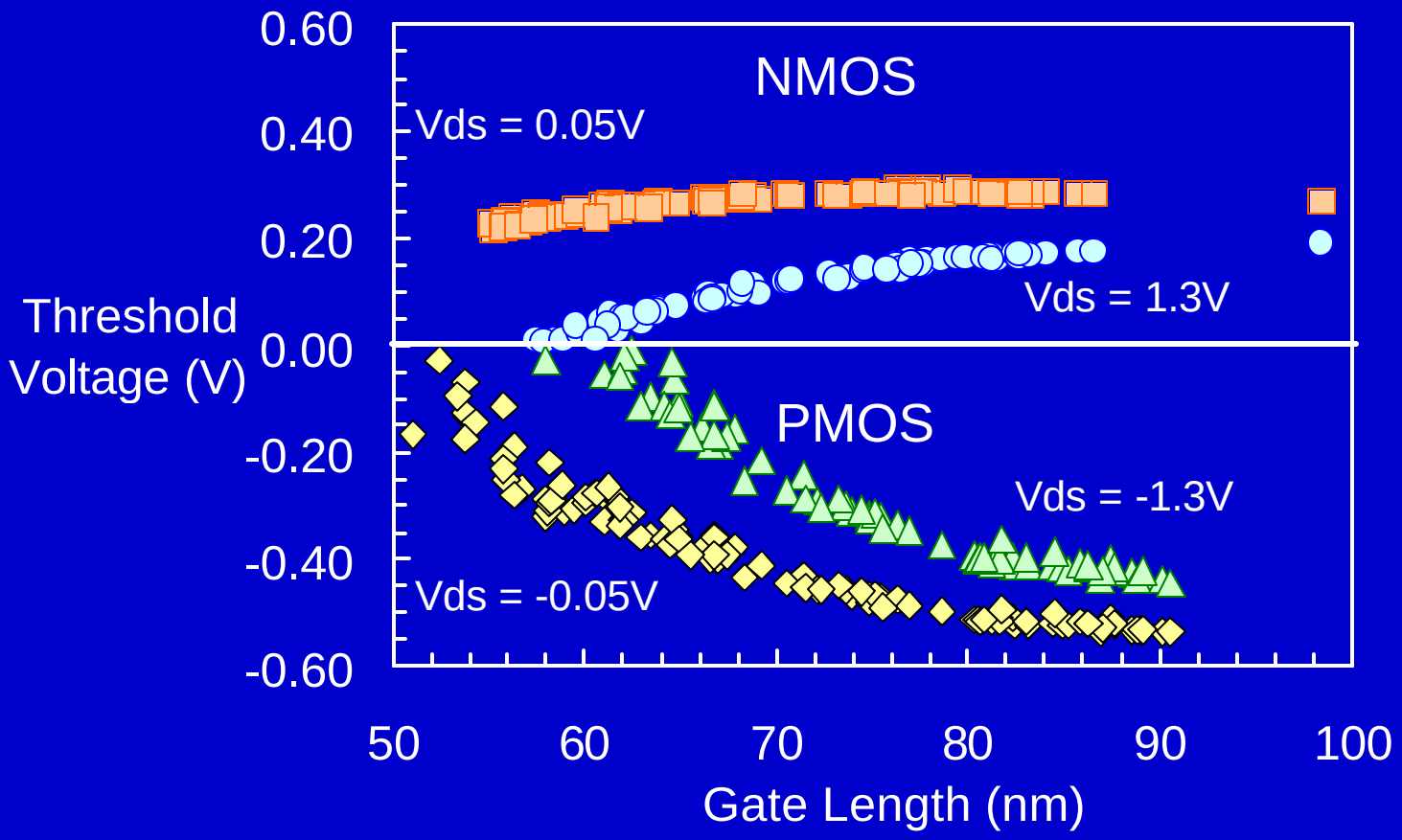
PMOS I_{DSAT} = -0.6 mA/mm NMOS I_{DSAT} = 1.17 mA/mm

High V_T Threshold Voltage vs. Gate Length



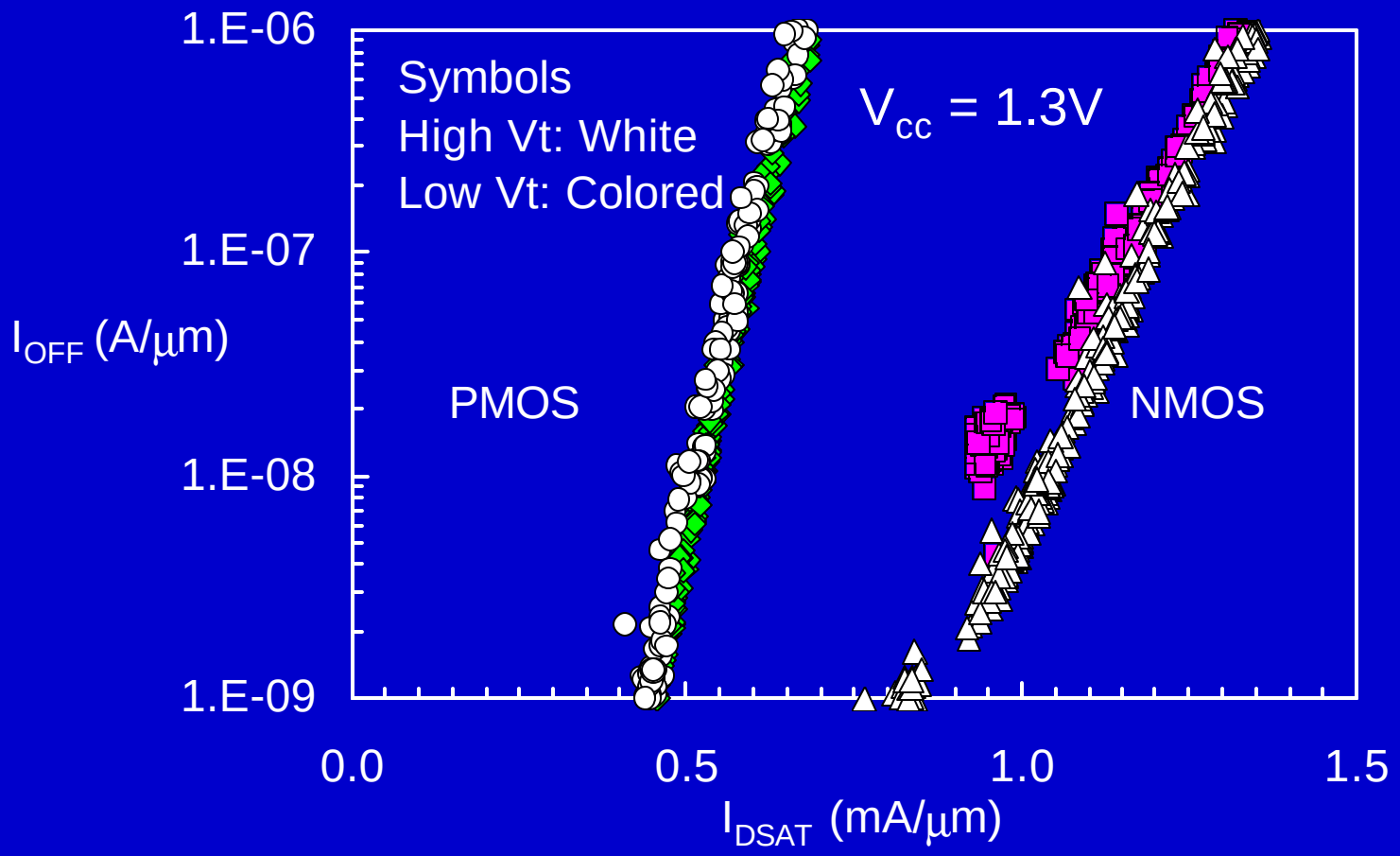
Excellent V_T roll off characteristics down to 60nm gate lengths

Low V_T Threshold Voltage vs. Gate Length



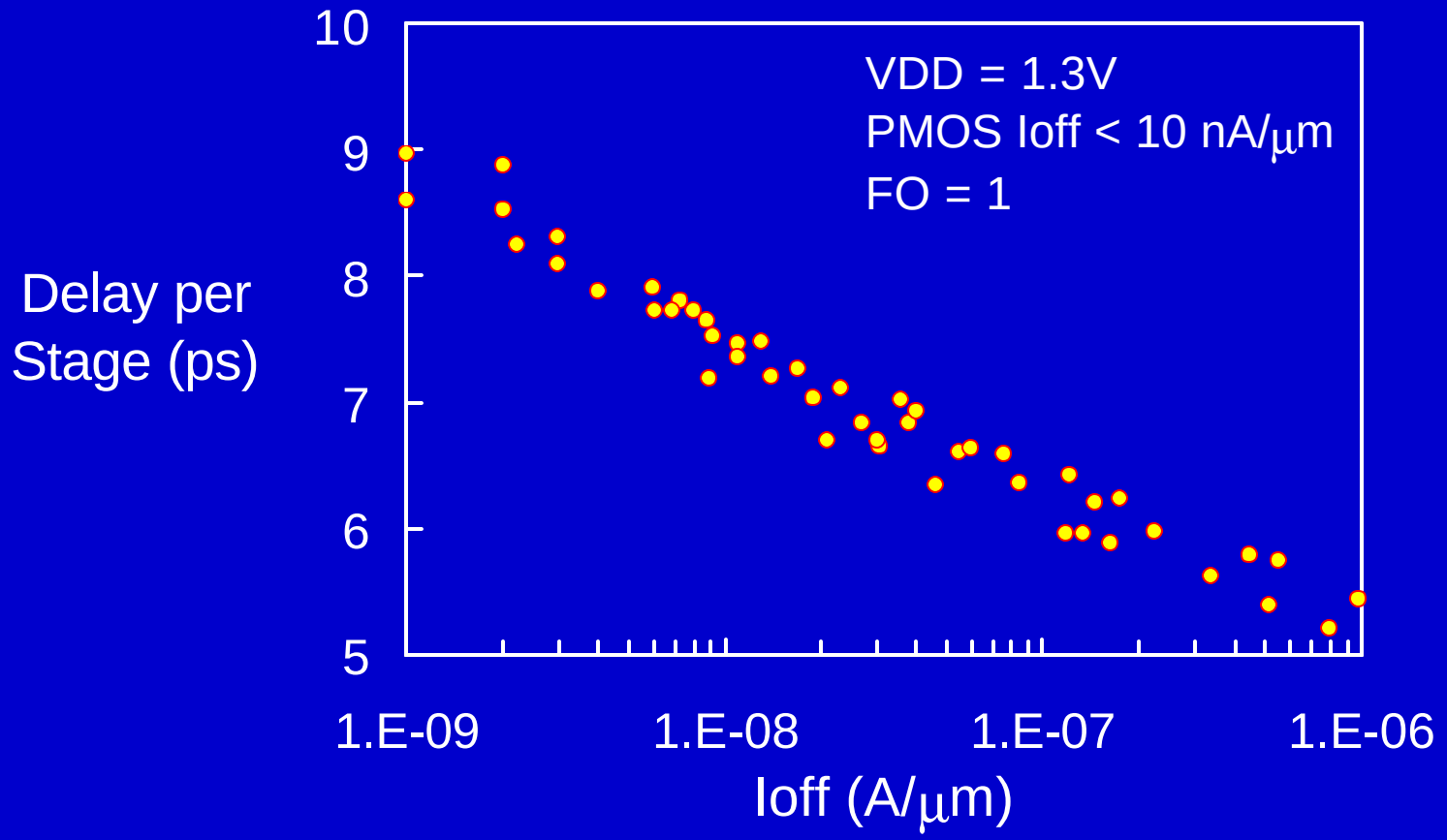
Excellent V_T roll off characteristics down to 60nm gate lengths

Drive Current vs. Off State Leakage



Best I_{ON}-I_{OFF} characteristics reported to date

Ring Oscillator Delay per Stage



7.5 ps delay for I_{OFF} = 10 nA/mm

6.5 ps delay for I_{OFF} = 100 nA/mm

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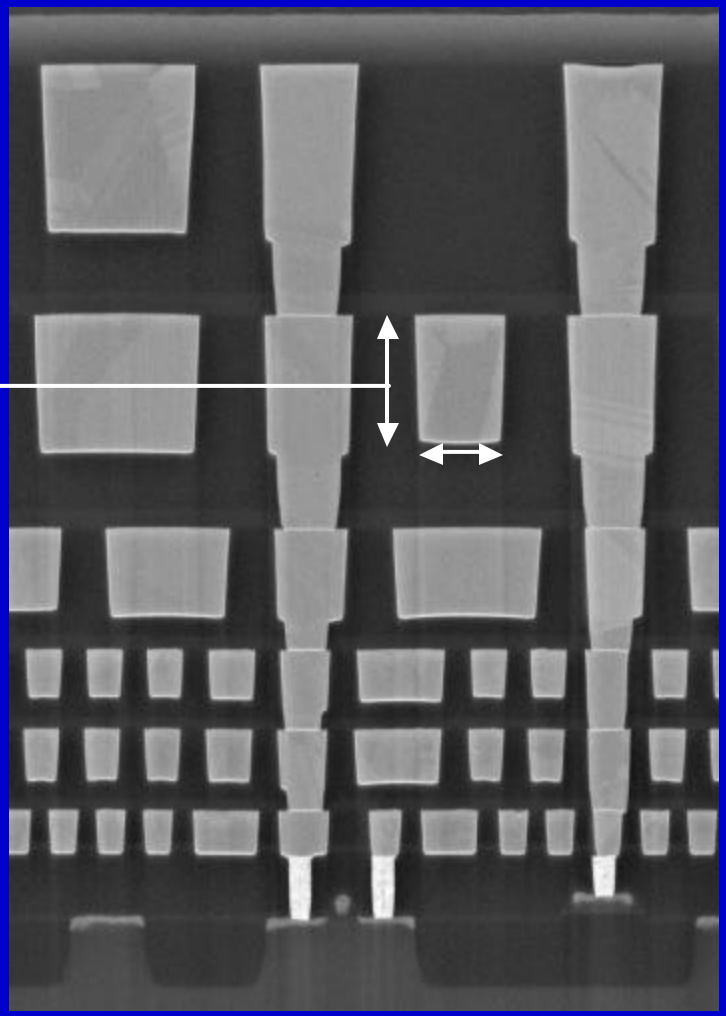
Damascene Copper Interconnects

Aspect Ratio
(T/W) = 1.6



Metal 6

Metal 5

Metal 4

Metal 3

Metal 2

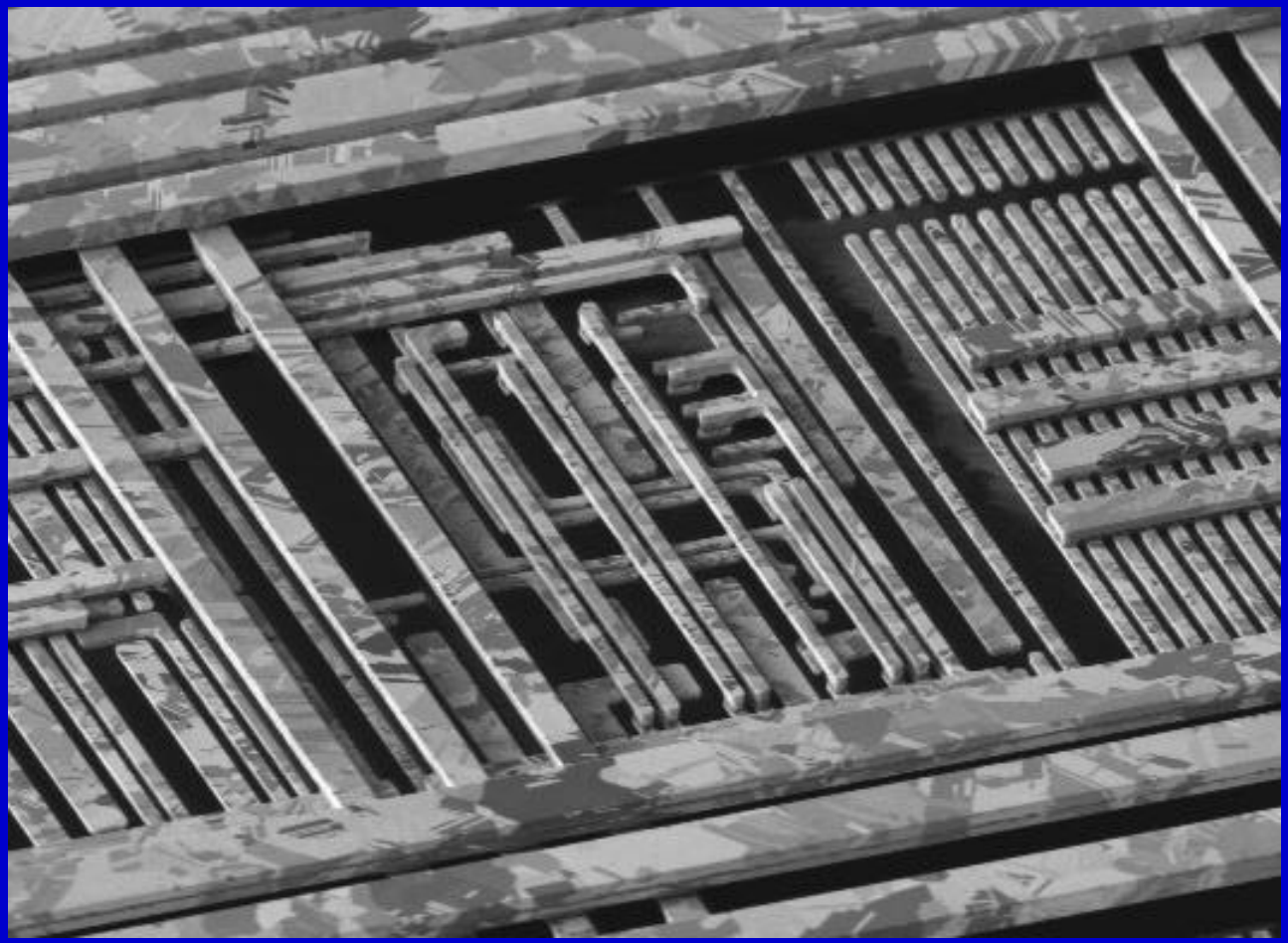
Metal 1

Transistors

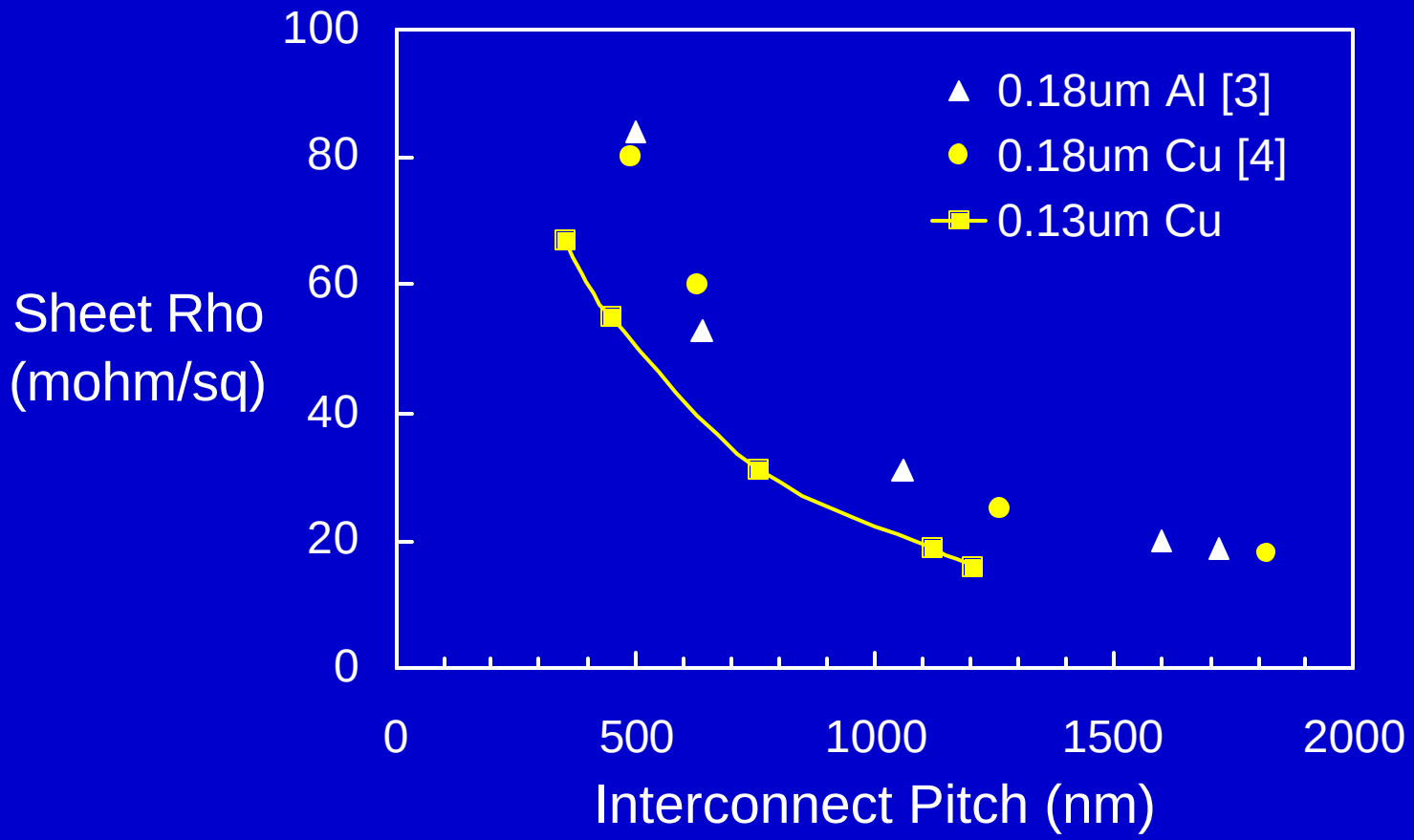
Interconnect Dimensions

Layer	Pitch	Thick	A.R.
Metal 1	350	280	1.6
Metal 2	448	360	1.6
Metal 3	448	360	1.6
Metal 4	756	570	1.5
Metal 5	1120	900	1.6
Metal 6	1204	1200	2.0
	nm	nm	

Damascene Copper Interconnects



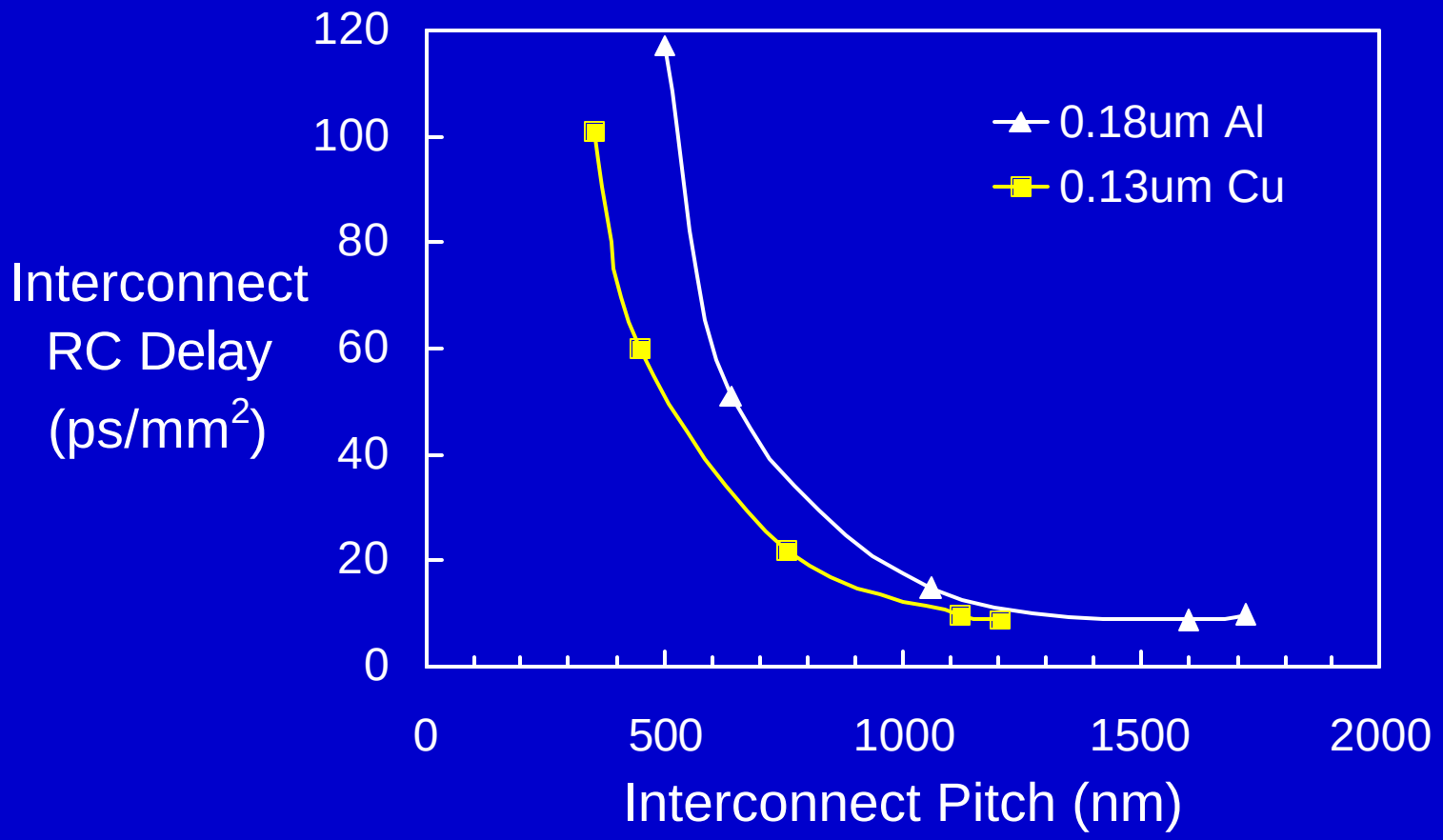
Interconnect Sheet Rho vs. Pitch



30% lower sheet rho at same pitch due to high aspect ratio copper

[3] Yang, 1998 IEDM [4] Crowder, 1999 VLSI Symposium

Interconnect RC Delay vs. Pitch



40% lower RC delay by using Cu + high aspect ratio + FSG ILD

intel

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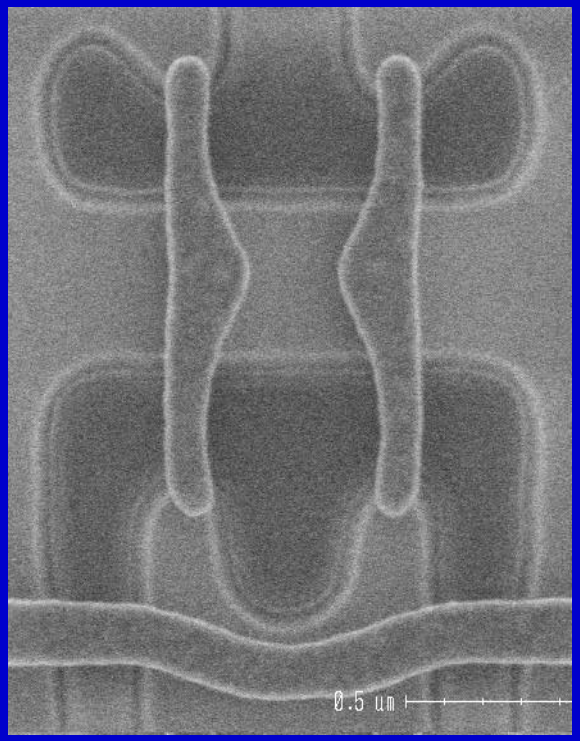
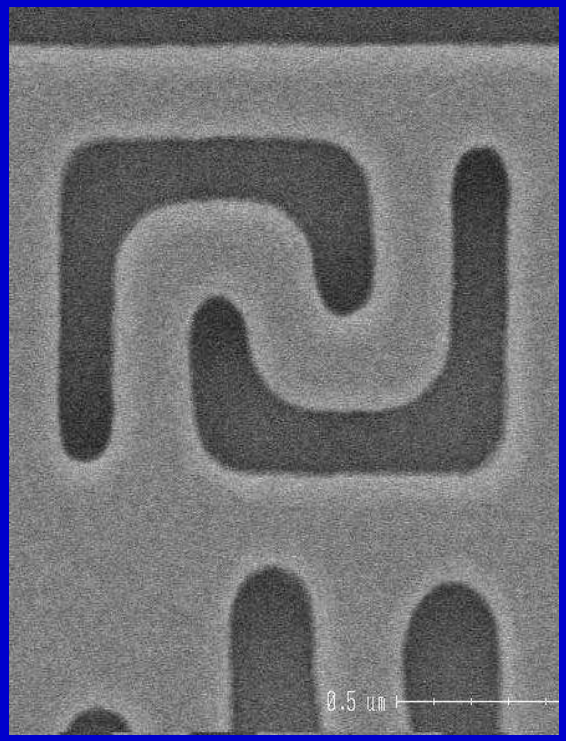
SRAM Features

- 18 Mbit CMOS SRAM
- >100 million transistors, 103 mm^2
- 2.45 μm^2 6-T SRAM cell
- SRAM used as yield, performance and reliability test vehicle during process development
- High yield and excellent performance demonstrated
- 2.09 μm^2 6-T SRAM cell developed using array-specific design rules

2.45 μm^2 6-T SRAM Cell



Poly over STI

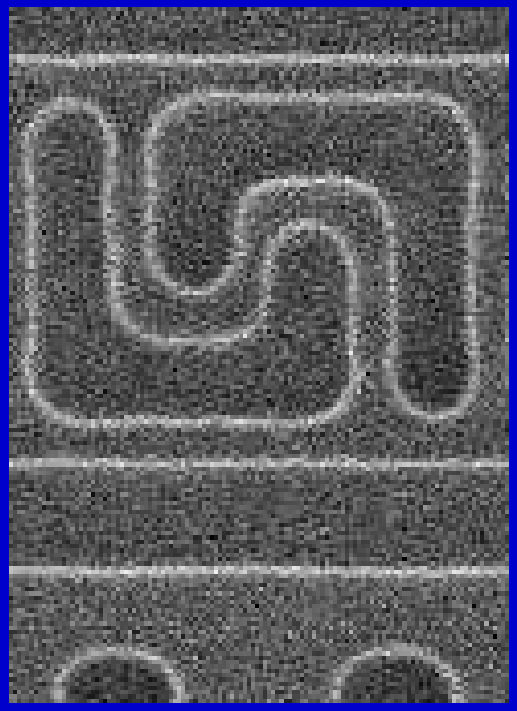


Metal 1

1.40 µm x 1.75 µm

2.09 μm^2 6-T SRAM Cell

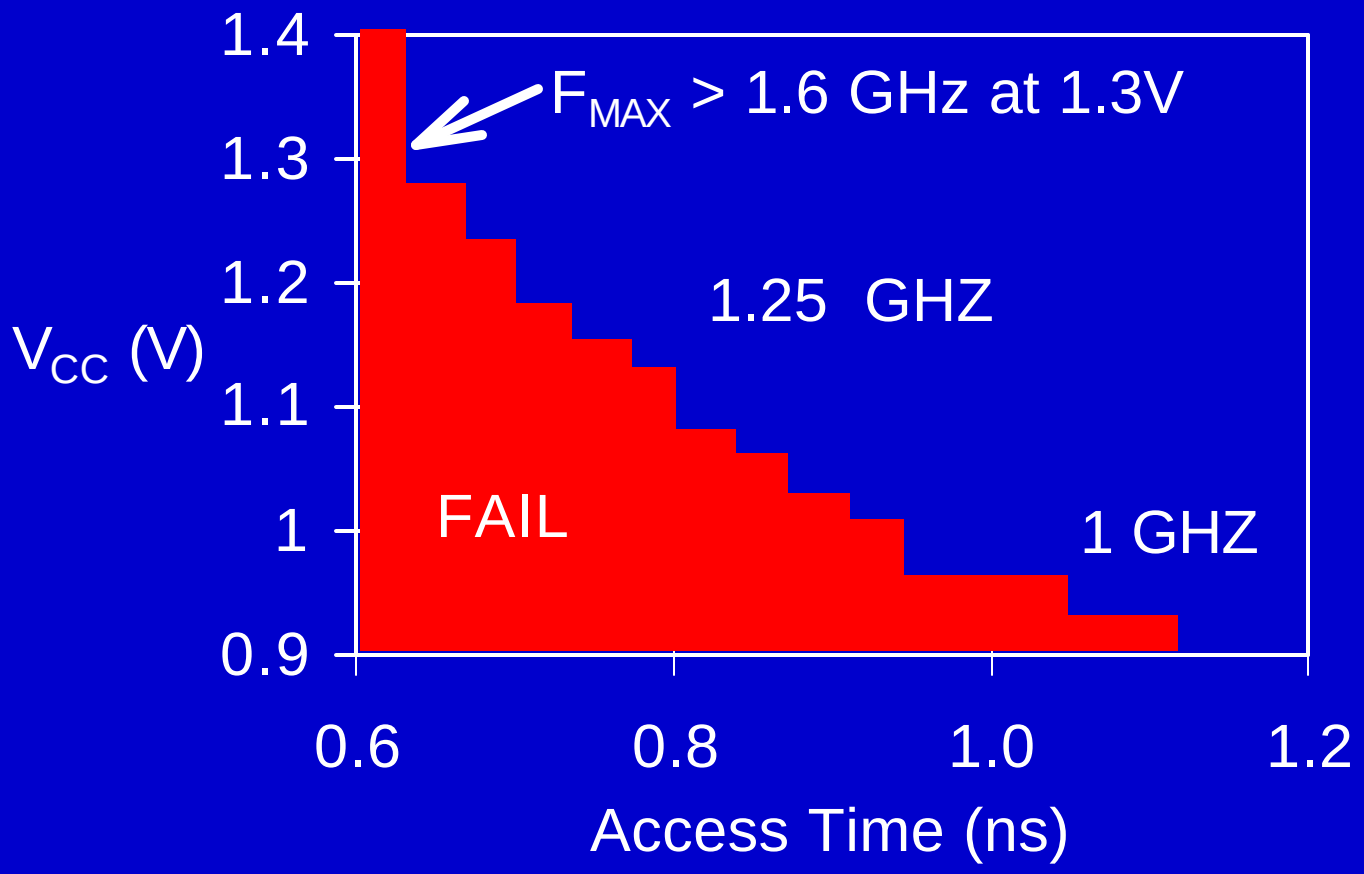
Poly over STI



Metal 1

1.23 µm x 1.69 µm

18 Mbit SRAM Performance



Conclusions

- A 130 nm logic technology has been developed
- High performance dual V_T transistors
  - 70 nm L_{GATE}
  - 1.5 nm gate oxide
  - Best reported I_{ON} vs. I_{OFF} characteristics at 1.3V
- High performance interconnects
  - 6 layers of high aspect ratio damascene copper
  - FSG low-k dielectric
  - 40% RC delay improvement
- Manufacturability demonstrated
  - 18Mb SRAM at >1.6 GHz
  - High yielding 130 nm generation microprocessors

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